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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,310	09/19/2001	Sung-min Yim	SEC.813	8171

7590 02/20/2003

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SUITE 150
12200 SUNRISE VALLEY DRIVE
RESTON, VA 20191

EXAMINER	
CHAN, EMILY Y	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 02/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,310	YIM ET AL.	
	Examiner	Art Unit	
	emily y chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to ~~communication(s)~~ Priority Paper filed on *19 September 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *1-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stambbaugh et al ('454) and further in view of Roberts et al ('661).

With respect to claims 1-2, 9 and 14-16, Stambbaugh et al ('454) teach semiconductor device test circuits and a method for determining fabrication parameters or measuring electrical characteristic of an electrical element within a packaged semiconductor device as clamed, comprising:

(1), connecting the electrical element (NCOMS transistor) of the semiconductor device to an electrical characteristic measurer (see Figs 3,and 6-9) that is connected to the electrical element (P-channel transistor 42, N-channel transistor44, 46) and a pad (28) of the semiconductor device, and that is driven in response to a control signal (test mode signal) to output a value that is indicative of the electrical characteristic of an electrical element to the pad (28) (see col.5, lines 25-26);

(2), controlling the semiconductor device to enter a predetermined electrical characteristic measuring mode (Fig 5, test mode detect circuit 76),

(3), generating a control signal (test signal) by a control signal generator or test mode circuit (76) that generates a control signal (test mode signal) and is activated in

an electrical characteristic measuring mode (see col.7, lines 66-68 and col. 8, lines 1-9); and

(4), driving the electrical characteristic measurer responsive to the control signal to provide a value indicative of the electrical characteristic of an electrical element to the pad (28) (see col.5, lines 25-26).

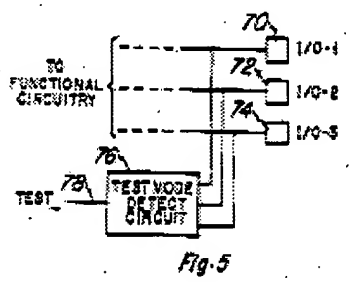

Fig.5

The difference between Stambbaugh et al ('454) 's teaching and the claimed invention is that Stambbaugh et al ('454) 's **control signal generator or test mode circuit** generates a test signal **in responsive to I/O pins of the semiconductor device** and the claimed **control signal generator** generates a test signal in responsive to **an address pin of the semiconductor device.**

Roberts et al ('661) disclose a method and apparatus relating to a test signal generator or a test signal switch control that is fabricated on a semiconductor die mounted in a semiconductor package (see col.2, lines 42-43) and expressly teach the operations of receiving an address signal and entering the electrical characteristic measurer mode for generating test signals in response to a value of at least one bit of the address signal received (See Fig 11, 100 below).

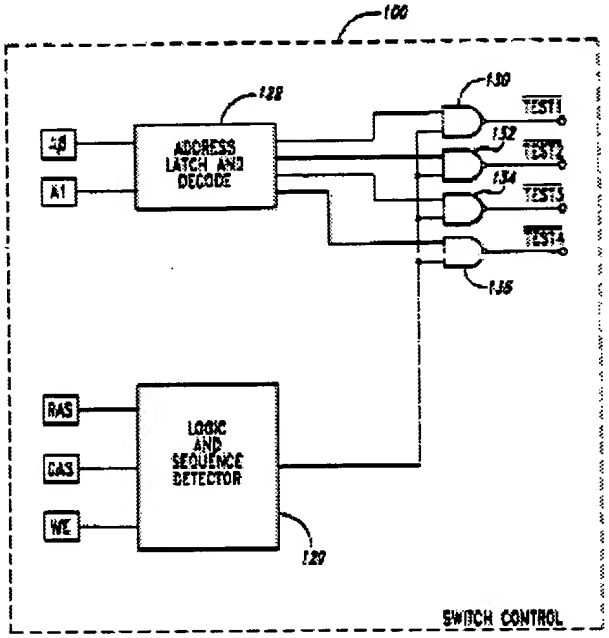

Fig. 11

It would have been obvious to one of ordinary skilled in the art at the time the invention was made to have substituted the Stambbaugh et al ('454) 's **control signal generator or test mode circuit** by Roberts et al ('661)'s test **switch circuit control** for generating test signals in responsive to a received address signal because both references are directed to test signal generation for measuring or testing electrical elements for packaged semiconductor device, and Stambbaugh et al ('454) 's and Roberts et al ('661)' s test signal generating circuit are functional equivalents as suggested by Roberts et al ('661) (see col. 6, lines 35-36, and col. 7, lines 49-51). Therefore, the substitution of functional equivalents in Stambbaugh et al ('454) would lead to the expected success.

With respect to claims 3 and 5-8 and 17, Stambbaugh et al ('454) teach that their electrical element is selected from a group including an NMOS transistor (see Fig 7), a PMOS Transistor (see Fig 8.) and a resistor (see col. 2, lines 29-30). Stambbaugh et al ('454) also teach the value that is Indicative of the threshold voltage and a saturation current of NMOS transistor, one of the threshold voltage and saturation current of the PMOS transistor and a resistance of the resistor (see col. 9, lines 21-68 and col. 10, lines 1-68).

With respect to claims 4, Stambbaugh et al ('454) teach that their electrical Characteristic measurer includes two same sizes of NMOS transistors (see Fig 7, 96 and 98) with structural connections be between them.

With respect to claim 10, Stambbaugh et al ('454) teach that their electrical element is one of a transistor and resistor , and the electrical characteristic measurer composing at least one transistor characteristic measurer unit and a resistor characteristic measuring unit that measures the electrical characteristic of the resistor, as selectable by the control signal (see col. 2, lines 24-30).

With respect to clams 11-12, Stambbaugh et al ('454) teach that their electrical Characteristics of the transistor are one of a threshold voltage and saturation current (See col. 9, lines 35-38) and their electrical characteristic of the resistor is a resistance (See col.10, lines 67-68).

With respect to claim 13, Roberts et al ('661) specifically teach that their test signal generator or test signal switch control (100) generates the control or test signal responsive only to **two bits** (a0 and a1) of the address signal (for claim 10).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Dreibelbis discloses semiconductor substrate test selection techniques and teaches to test integrated circuits formed on the semiconductor substrate.

Dalrymple et al disclose a bus-oriented integrated circuit chip testing system and teach test mode circuit for generating test signal in response to received address signals.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily y Chan whose telephone number is 7033056123. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Cuneo Kammie can be reached on 7033081233. The fax phone numbers for the organization where this application or proceeding is assigned are 7033085841 for regular communications and 7033085841 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 7022056123.

KAMAND CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ec
February 10, 2003